A1280H

Uncooled Thermal Imaging Module

Product Manual

V1.0.0

Historical Versions

Version	Date	Description
V1.0.0	2024-08	Initial release

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1 Product Description

The A1280H uncooled thermal imaging module, with 1280×1024 resolution, features light weight, compact size, and low power consumption. It is suitable for micro unmanned aerial vehicle (UAV) systems, various small handheld telescopes, helmet night vision devices, multi-spectrum fusion googles and other optoelectronics. High-reliability design, it has good vibration and shock resistance to meet the needs of products with high-reliability requirements, such as electro-optical payloads, vehicle-mounted applications, and scopes. Supporting multiple communication protocols and video output formats, it offers infrared lenses with varied specifications for diversified applications.

2 Len Type

Table 2.1 Lens Parameters

Array Size	Focal Length/F#	Lens type	HFOV×VFOV	IFOV
1280×1024	19mmF1.0	Athermalized	46.4°(H)×37.1°(V)	0.63mrad
	25mmF1.0	Athermalized	35.3°(H)×28.2°(V)	0.48mrad
	35mmF1.0	Athermalized	25.1°(H)×20.1°(V)	0.34mrad
	50mmF1.0	Athermalized	17.46°(H)×14.01°(V)	0.24mrad
	55mmF1.0	Athermalized	16.0°(H)×12.8°(V)	0.22mrad
	75mmF1.0	Athermalized	5.9°(H)×4.7°(V)	0.16mrad

3 Product Performance Parameters

Table 3.1 Specifications [1]

Performance Indicators	
Detector Type	Uncooled VOx infrared detector
Resolution	1280×1024
Pixel Pitch	12μm
Detector Frame Rate	30Hz
Spectral Band	8~14μm
NETD	≤40mK@25℃, F#1.0
MRTD	≤400mK@25°C, F#1.0, 55mm lens
Thermal Time Constant	≤15ms
Non-uniformity Correction	Support TECLESS algorithm

Self-checking Time	≤8s
Startup Time [2]	≤15s (HDMI<20s)
Single Point Calibration Time [3]	≤1.5s
Image Delay [4]	≤5ms
Image Non-uniformity	σ≤15/1%
Function Indicators	
Self-checking Function [5]	Power-on self-checking and instruction self-checking available
Brightness&Contrast Adjustment	Auto/manual(Auto by default)
Polarity	Black-hot/white-hot (default)
Color Palettes	Support[2]
Reticle	Display/blank (default)/move (digital video)
Digital Zoom	8×
Image Processing	NUC
	DNR
	DDE
Mirroring [6]	Horizontal/Vertical/Diagonal
Image Correction	Auto/manual/background correction is available, with a function to disable auto correction
External Synchronization Function	Self-synchronization (default)/internal synchronization/external synchronization/adaptive synchronization mode
Shutter	Bistable shutter
Shutter Normally Closed	With the function of shutter normally closed (enabled by default)
Serial Port Firmware Upgrade	Firmware upgrade through serial port available
Electrical Parameters	
Input Supply Voltage	6-20V
Typical Supply	6V
Typical Power Consumption (Without Expansion Board)	Steady status ≤ 1W
Insulation Protection	The enclosure ground is insulated from signal and power ground with an insulation resistance of >10MΩ
Interface Parameters	

Video Output	Analog Video	None
	Digital Video	Cameralink/BT1120/HDMI/USB
Serial Communication Interface		RS422
External Synchronization		LVTTL
Physical Characteristics		
Dimensions (Without Lens and Extension Components)		32×32×25.5mm
Weight (Without Lens and Extension Components)		43g±5g
Environment Adaptability		
Operating Temperature		-40℃~+60℃
Storage Temperature		-45℃~+70℃
Vibration		6.06g, random vibration, three axes, 5min/axis
Shock		1000g@0.3ms, optical axis direction

Notes:

(1) Ambient test environment: temperature: 23 to 25 ℃, humidity: 50 to 55%RH, and standard atmospheric pressure: 101.325kPa;

(2) To solve the image stability, after the module is powered on,, the current status is set to the initial status, and automatic shutter correction can be triggered when the following 3 conditions are met:

① The internal timer exceeds the set shutter correction interval, which defaults to 10 min;

② Changes in the ambient temperature of the module above a set threshold, which defaults to 5℃;

③ The detector focal plane temperature change exceeds a set threshold, which defaults to 2℃.

Notes:

④If one of the three conditions above triggers the shutter correction, the initial status is changed to

⑤the current status, from which the detection of the above 3 conditions continues;

(3) Single-point calibration time refers to the time from when the shutter instruction is issued to when the instruction return value is received;

(4) Image delay: The image delay due to the algorithm does not include the image delay of the detector. The shortest delay, when used with the Cameralink interface, is described in detail in Section 7;

(5) Self-checking enables self-checking of detectors, FLASH, DDR, and temperature sensors;

(6) There are two methods available: a. Flip the device through instructions. For back-end processing, frames need to be cached, and the image delay is increased by 2 frames. b. Return the device to the factory for re-correction.

4 Description of Module Component Interface

4.1 Interface Pinout

Hardware interface socket model: DF40C-70DP-0.4V (51)

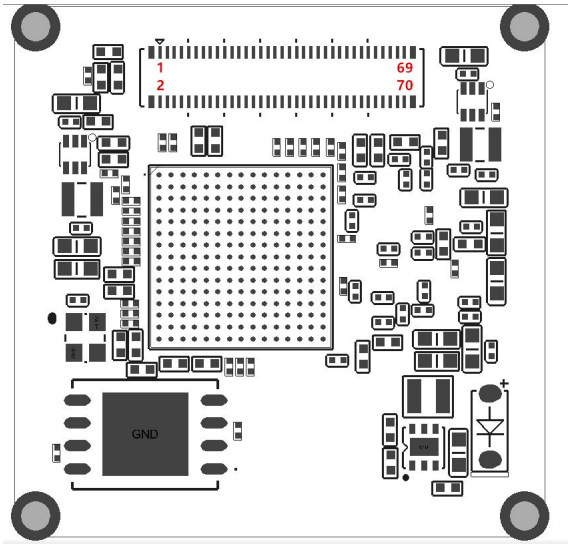


Figure 4.1 Interfaces Without Extension Components

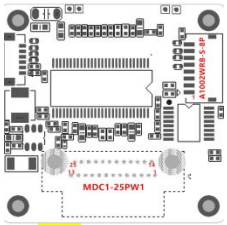
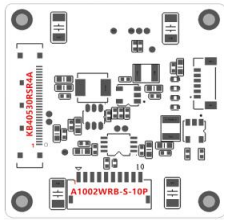
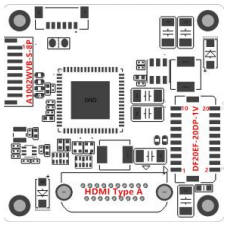
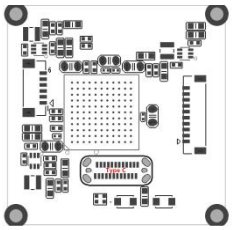
Table 4.1 Definition of Interfaces Without Extension Components

Pin No.	Pin Name	Type	Description
1	VCC	Power supply	Power input (5.0V DC)
2	VCC	Power supply	Power input (5.0V DC)
3	VCC	Power supply	Power input (5.0V DC)
4	VCC	Power supply	Power input (5.0V DC)
5	NC	/	Unused
6	NC	/	Unused
7	NC	/	Unused
8	NC	/	Unused
9	GND	Power supply	Power GND
10	GND	Power supply	Power GND
11	GND	Power supply	Power GND
12	GND	Power supply	Power GND

Pin No.	Pin Name	Type	Description
13	UART_RX	Input	Serial port input (3.3V)
14	UART_TX	Output	Serial port output (3.3V)
15	NC	/	Unused
16	NC	/	Unused
17	NC	/	Unused
18	NC	/	Unused
19	GND	Power supply	Power GND
20	GND	Power supply	Power GND
21	GND	Power supply	Power GND
22	GND	Power supply	Power GND
23	NC	/	Unused
24	NC	/	Unused
25	NC	/	Unused
26	NC	/	Unused
27	GND	Power supply	Power GND
28	GND	Power supply	Power GND
29	DV0	Output	DATA0 (1.8V)
30	DV1	Output	DATA1 (1.8V)
31	DV2	Output	DATA2 (1.8V)
32	DV3	Output	DATA3 (1.8V)
33	DV4	Output	DATA4 (1.8V)
34	DV5	Output	DATA5 (1.8V)
35	DV6	Output	DATA6 (1.8V)
36	DV7	Output	DATA7 (1.8V)
37	DV8	Output	DATA8 (1.8V)
38	DV9	Output	DATA9 (1.8V)
39	DV10	Output	DATA10 (1.8V)
40	DV11	Output	DATA11 (1.8V)
41	DV12	Output	DATA12 (1.8V)

Pin No.	Pin Name	Type	Description
42	DV13	Output	DATA13 (1.8V)
43	DV14	Output	DATA14 (1.8V)
44	DV15	Output	DATA15 (1.8V)
45	FRAME_VALID	Output	Frame valid (1.8V)
46	LINE_VALID	Output	Line valid (1.8V)
47	SYNC	Input/Output	Synchronization signal (3.3V)
48	CLK	Output	Clock signal 1.8V
49	GND	Power supply	Power GND
50	GND	Power supply	Power GND
51	NC	/	Unused
52	NC	/	Unused
53	NC	/	Unused
54	NC	/	Unused
55	GND	Power supply	Power GND
56	GND	Power supply	Power GND
57	NC	/	Unused
58	NC	/	Unused
59	NC	/	Unused
60	NC	/	Unused
61	NC	/	Unused
62	NC	/	Unused
63	NC	/	Unused
64	NC	/	Unused
65	GND	Power supply	Power GND
66	GND	Power supply	Power GND
67	GND	Power supply	Power GND
68	GND	Power supply	Power GND
69	GND	Power supply	Power GND
70	GND	Power supply	Power GND

4.2 List of User Extension Component

Model	Figure	Main Interfaces/Functions	Compatible Modules
TAH04V100F008C		• Power Input: 5–20 VDC, typical voltage 12 VDC • Communication: RS422 • CameraLink Digital Video • External Synchronization Interface • Motor Control: RS422 • Power Output: 5–18 VDC	1280
TAH04V100F027C		• Power Input: 5–18 VDC, typical voltage 12 VDC • Communication: UART • BT1120 Digital Video • External Synchronization Interface • Motor Control: RS422 • Power Output: 5–18 VDC	1280
TAH04V100F015C		• Power Input: 5–18 VDC, typical voltage 12 VDC • Communication: RS422 * 2, RS232 • HDMI Type A Interface • External Synchronization Interface • Motor Control: RS422 • Power Output: 5–18 VDC	1280
TAH04V100F016		• Power Supply: USB-powered, typical voltage 5 VDC • Communication: USB • USB UVC Digital Video	1280

4.3 LVCMOS Digital Video (30Hz)

LVCMOS usually refers to a level standard for digital signals and, in this case, a digital video format. LVCMOS digital video contains 1 clock signal line, 1 frame synchronization (field synchronization) signal line, 1 line synchronization signal line, 1 enable signal line, and 14 parallel data signal lines. When a data frame arrives, the frame synchronization signal goes high, indicating that the next data is the same data frame. When the frame is finished, the frame synchronization signal goes low, indicating the end of the data frame. Similarly, when a line of data arrives, the line synchronization signal goes high, and when the line of data is finished, the line synchronization signal goes low.

The A1280H outputs the LVCMOS video at 30Hz, as shown below:

Table 4.2 LVCMOS Clock Frequency

Product Model	Clock Frequency
A1280H	42.5MHz

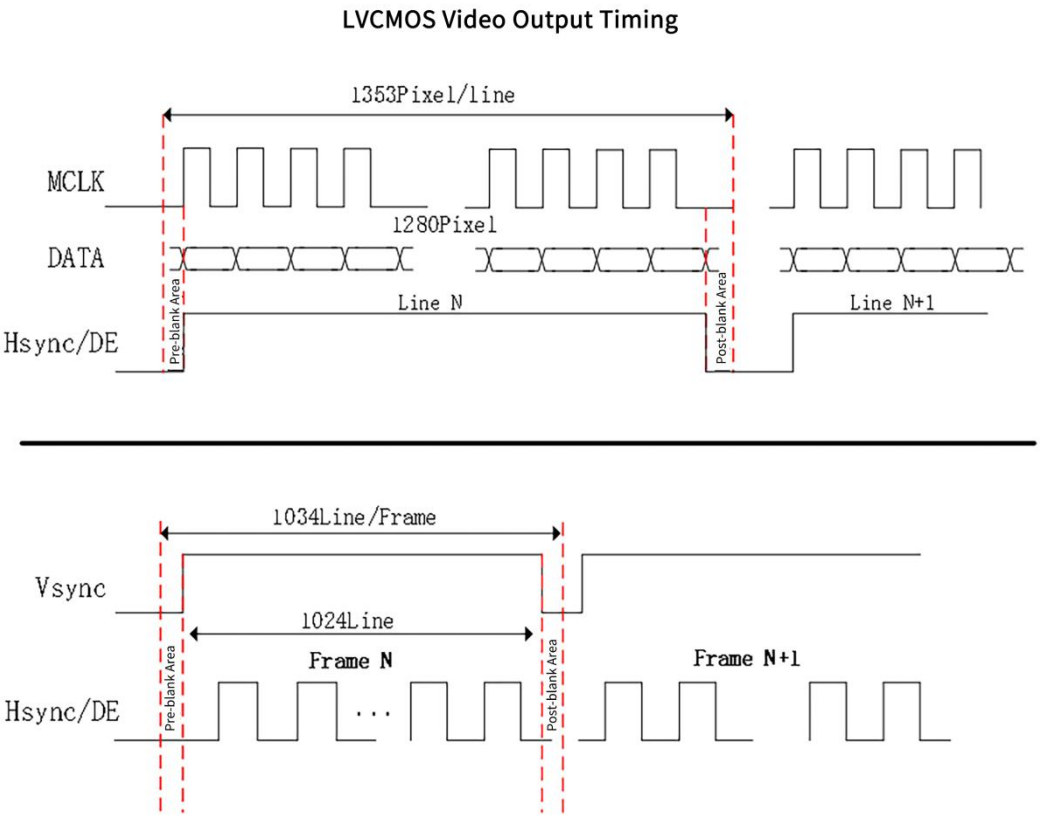


Figure 4.2 LVCMOS Timing Diagram

Table 4.3 LVCMOS Timing Description

No.	Signal	Description	Remarks
1	MCLK	Clock	42.5MHz (=1353×1034×30Hz)
2	DATA	Data	Valid data: 1280 pixels×1024 lines
3	Hsync	Line synchronization	There are 1353 pixels in one line, of which 1280 are valid data, and the remaining 73 are blanking data; there are 11 pixels in the pre-blanking area and 62 pixels in the post-blanking area.
4	Vsync	Frame synchronization	There are 1034 lines in one frame, 1024 of which are valid data lines, and the remaining 10 are blanking data lines.
5	DE	Enable	Consistent with Hsync

Each pixel of digital video data corresponds to 1 clock cycle. The amount of data per frame is the same as the module detector's area array size, which is 1280×1024, and each LVCMOS frame contains 1280×1024 = 1310720 pixels of data, with 1280 data bits per line, for a total of 1024 lines. Each line synchronization signal goes high for 1280 clock cycles, and the line synchronization signal is set high 1024 times during a data frame. In the above diagram, the synchronization signal and the data signal are changed at the clock's rising edge. In the actual programming, the signal can be made to start changing at the falling edge of the clock so that the receiver can sample at the rising edge of the clock. The above timing is for reference only.

4.4 BT1120 Digital Video

BT1120 digital video is output in YCbCr color format with a serial data width of 16-bit, brightness in high 8-bit, chrominance in low 8-bit, and brightness and chrominance output in the same clock cycle. The standard BT1120 format of 1080p@30Hz is used, with a clock frequency of 74.25MHz and a frame rate of 30Hz, with 2200 pixels per line and 1125 lines in total, i.e., 2200×1125×30Hz = 74.25MHz.

Table 4.4 BT1120 Clock Frequency

Product Model	Clock Frequency
A1280H	74.25MHz

The data format is shown in Table 6. The line direction 0-40 and 1121-1124, that is, the first 41 lines and the last 4 lines are blanking lines, and 41-1120, that is, the middle 1080 lines are valid lines. The column direction 4-275 is blanking columns, 0-3 is the video end reference code EAV, 276-279 is the video start reference code SAV, and 280-2199 that is, the last 1920 columns are valid columns. On the blank line, EAV corresponds to FFFF, 0000, B6B6, SAV corresponds to FFFF, 0000, ABAB, and the blank column corresponds to the valid column 8010; on the valid line, EAV corresponds to FFFF, 0000, 9D9D, SAV corresponds to FFFF, 0000, 8080, and the blank column corresponds to 8010. The valid column corresponds to the valid data.

Table 4.5 BT1120 Standard 1080P@30Hz Data Format (Hexadecimal)

Number of Columns / Number of Lines	0	1-2	3	4-275	276	277-278	279	280-2199
0-40	FFFF	0000	B6B6	8010	FFFF	0000	ABAB	8010
41-1120	FFFF	0000	9D9D	8010	FFFF	0000	8080	DATA
1121-1124	FFFF	0000	B6B6	8010	FFFF	0000	ABAB	8010

In summary, this format supports a maximum of 1920×1080 valid output; the A1280H actual valid output is 1280×1024, shown in the center, with the rest of the data filling in the black border. The data format is

shown in Table 4.6. The 41-1120 in the line direction corresponds to valid lines, where 69-1092 corresponds to actually valid lines (1024 lines), and 41-68 and 1093-1120 correspond to vertical blanking lines (28 lines for each); The 280-2199 in the column direction corresponds to valid columns, where 600-1879 corresponds to actually valid columns (1280 columns), and 280-599 and 1880-2199 correspond to the horizontal blanking columns (320 columns for each). The blank lines and columns correspond to 8010.

Table4.6 BT1120 Actual Valid Data Output Format (Hexadecimal)

Number of Columns / Number of Lines	0	1-2	3	4-275	276	277-278	279	280-599	600-1879	1880-2199
0-40	FFFF	0000	B6B6	8010	FFFF	0000	ABAB	8010	8010	8010
41-68	FFFF	0000	9D9D	8010	FFFF	0000	8080	8010	8010	8010
69-1092	FFFF	0000	9D9D	8010	FFFF	0000	8080	8010	DATA	8010
1093-1120	FFFF	0000	9D9D	8010	FFFF	0000	8080	8010	8010	8010
1121-1124	FFFF	0000	B6B6	8010	FFFF	0000	ABAB	8010	8010	8010

Note: *During the self-development of BT1120 user board, please note that given the high clock rate and high wire loss in some cables, it is recommended to add a 1.8V pull-up resistor to the clock pin of the user board.*

4.5 Description of Synchronization Mode

The module works at the corresponding frequency according to the set synchronization mode with a frequency range of 20-30Hz; the module's external synchronization signal pin EXT_SYNC can input the external synchronization signal or output the module internal synchronization signal according to the set synchronization mode. If EXT_SYNC is used as an output, the module outputs a fixed frequency clock signal; if EXT_SYNC is used as an input, an external clock signal is required, LVCMOS level, frequency within 20-30Hz, rising edge trigger.

Table 4.7 Description of Synchronization Mode

Synchronization Mode	Module Operating Mode	Pin Status	Frequency
Self-synchronization	Module Self-synchronization	High resistance	30Hz
Internal Synchronization	The module synchronizes itself and outputs the internal synchronization signal	Output	30Hz
External Synchronization	Module receives external synchronization signal	Input	20-30Hz

Adaptive	Module synchronizes itself when no external synchronization signal is input; the module works according to the external synchronization trigger signal when an external synchronization signal is input	Input	30Hz for internal synchronization, and 20-30Hz for external synchronization

The module is self-synchronized, i.e., it works continuously at a set frequency and outputs images without being influenced by other external devices; the module works according to the external synchronization trigger signal, i.e., it receives an external clock signal (LVCMOS level, frequency within 20-30Hz, rising edge trigger) before it starts to work and outputs a frame of image and then waits for the next trigger signal.

The module works in self-synchronization mode by default. For the use of the synchronization function, the synchronization mode can be changed via the serial port as required. The device on which the synchronization signal occurs must share ground with the module signal ground when EXT_SYNC is in an input status. The module conversion instructions are shown in Table 4.8.

Table 4.8 Conversion Instructions of Module Synchronization Mode

Mode	Head	Bytes	Instruction Set	Word	Operation Word	Mode	Frequency	Checksum	Tail	
Self-synchronization	AA	06	01	A3	01	00	00	55	EB	AA
Internal Synchronization	AA	06	01	A3	01	01	00	56	EB	AA
External Synchronization	AA	06	01	A3	01	02	00	57	EB	AA
Adaptive	AA	06	01	A3	01	03	00	58	EB	AA

Precautions:

(1) The synchronization mode is set to external synchronization. The external trigger signal frequency, independent of the frequency byte in the instruction, determines the actual frequency.

(2) The synchronization mode is set to external synchronization. Only when external synchronization setting instructions are sent external trigger signals can be provided for normal imaging, or there is no image output.

(3) The external input trigger signal should use the square signal.

(4) In the module conversion instruction, the "mode" bit is modified to switch between different modes; the "frequency" bit is not used and is written as 00 by default.

In internal synchronization mode, the corresponding timing of the output internal synchronization signal is as follows:

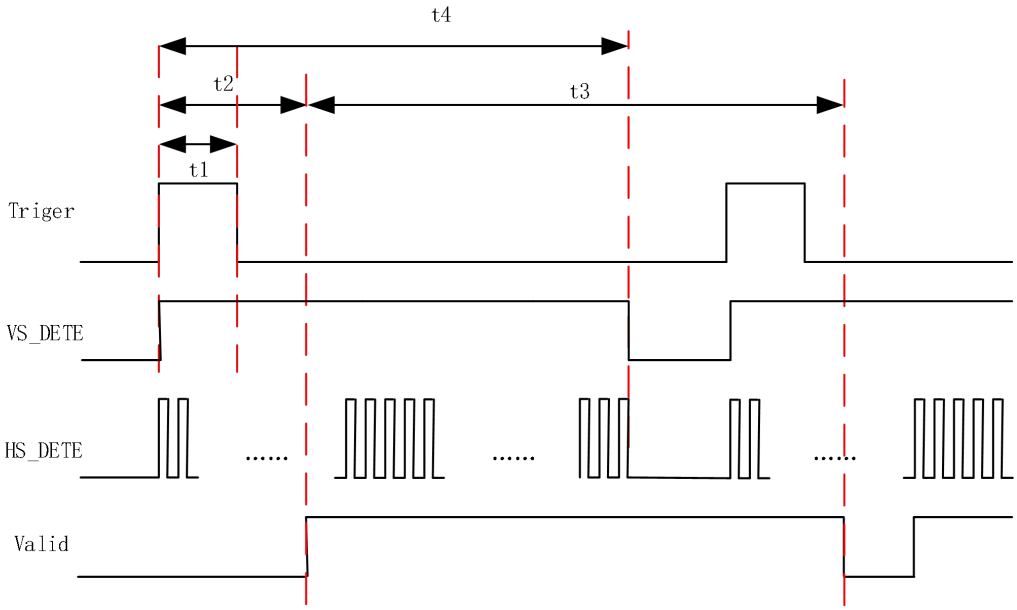


Figure 4.3 Internal Synchronization Timing Diagram

Table 4.9 Internal Synchronization Timing Description

Name	Date
t1: Pulse signal time	4ms
t2: Interval between pulse and digital video output	≤5ms
t3: Valid digital video output time	32.59ms
t4: Valid detector output time	32.59ms

Notes:

(1) The Triger in the figure is the output synchronization signal; VS_DETE and HS_DETE are the signals at the detector side; Valid is the valid signal of the image processing completion output;

(2) t1 is the pulse signal duration, with an error of ±0.05ms;

(3) t2 is the pulse and digital video output interval, here according to the LVCMOS digital video direct output format, the specific time to the actual video format shall prevail;

(4) t3 is the digital video valid output time, corresponding to the digital video continuous output time of one frame (1024 lines) of valid data, with an error of ± 0.05ms;

(5) t4 is the detector's valid output time, corresponding to the time for the detector to continuously output one frame (1024 lines) of valid data, with an error of ± 0.05ms.

4.6 Description of Image Algorithm Processing Delay

The A1280H digital video output can be split into two types: direct output and support for zoom output, as shown in Figure 4.4.

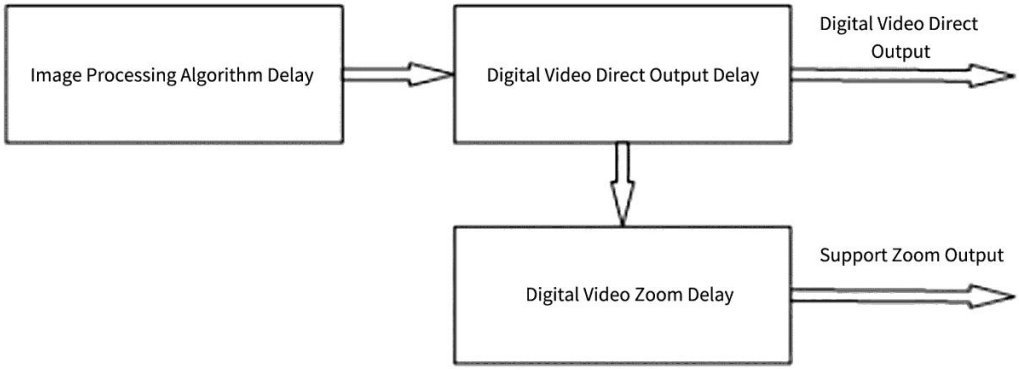


Figure 4.4 Schematic Diagram of Digital Video Output

1. Image processing algorithm delay: ≤5ms
2. Digital video direct output delay: =0ms
3. Digital video zoom delay: ≤66.6ms (two frames)

The digital video direct output delay is ≤5ms; the zoom output delay is ≤71.6ms.

5 Structures and Dimensions

5.1 Structures and Dimensions of Module with Cameralink Extension Component

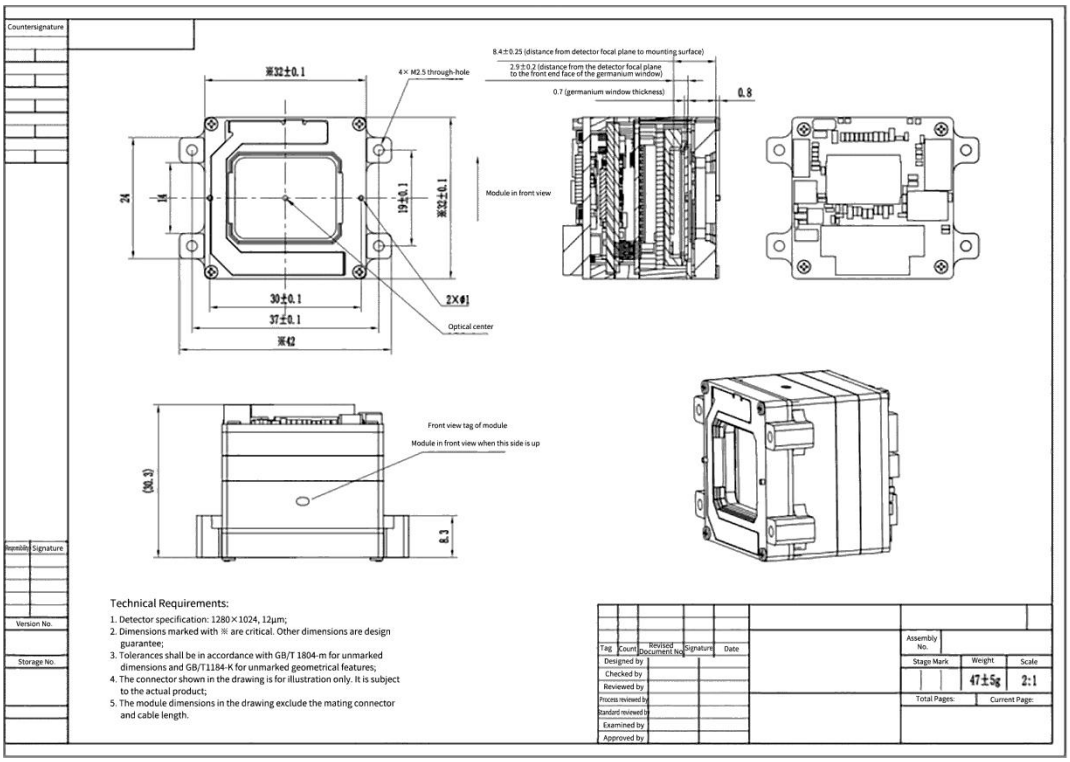


Figure 5.1 Module Structure with Cameralink Extension Component

5.2 Structure of BT1120 Extension Component

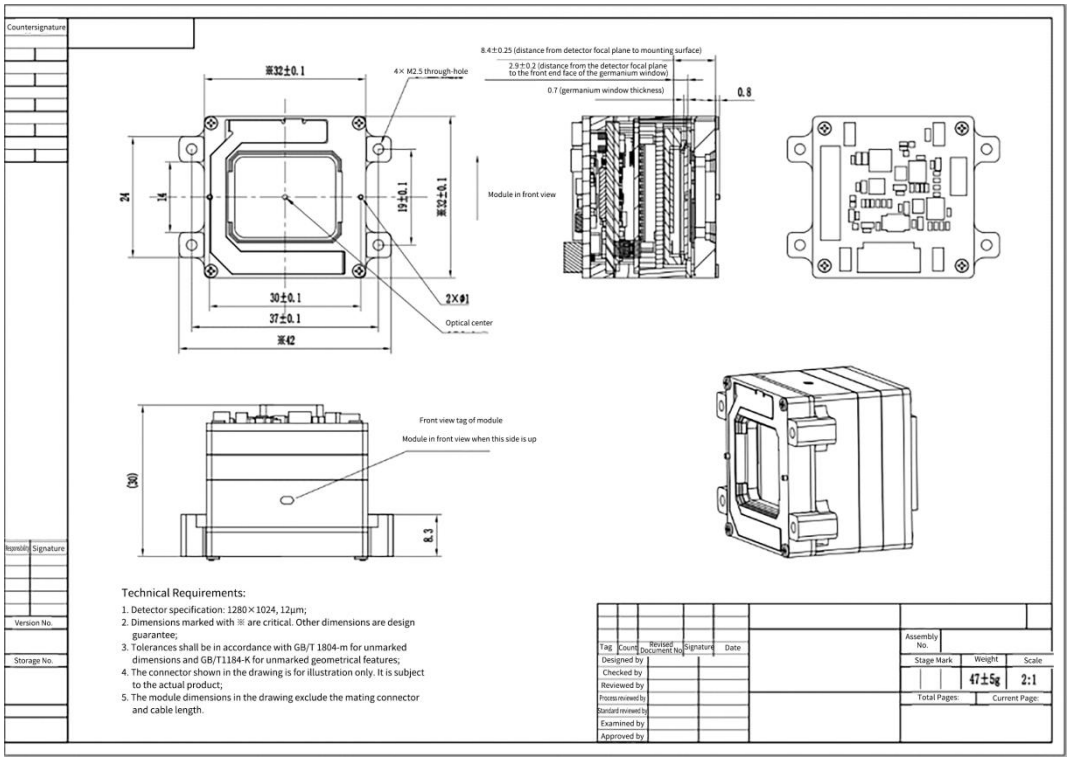


Figure 5.2 Module Structure with BT1120 Extension Component

5.3 Structure of HDMI Extension Component

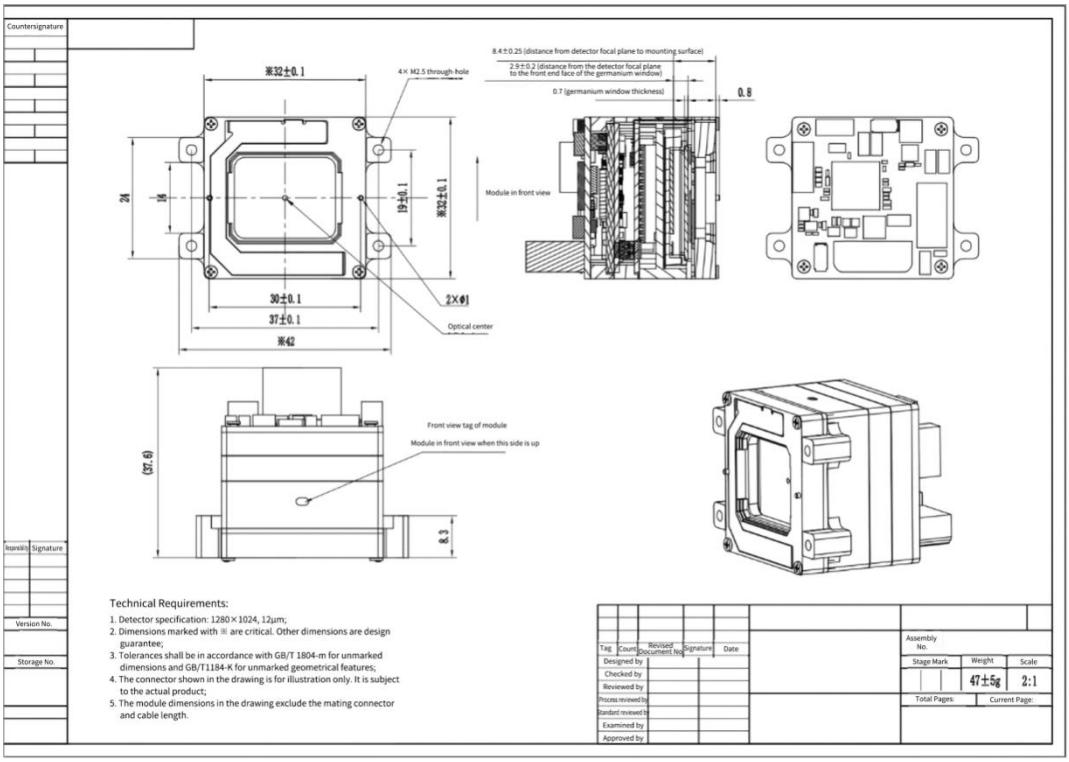


Figure 5.3 Module Structure with HDMI Extension Component

5.4 Structure of USB Extension Component

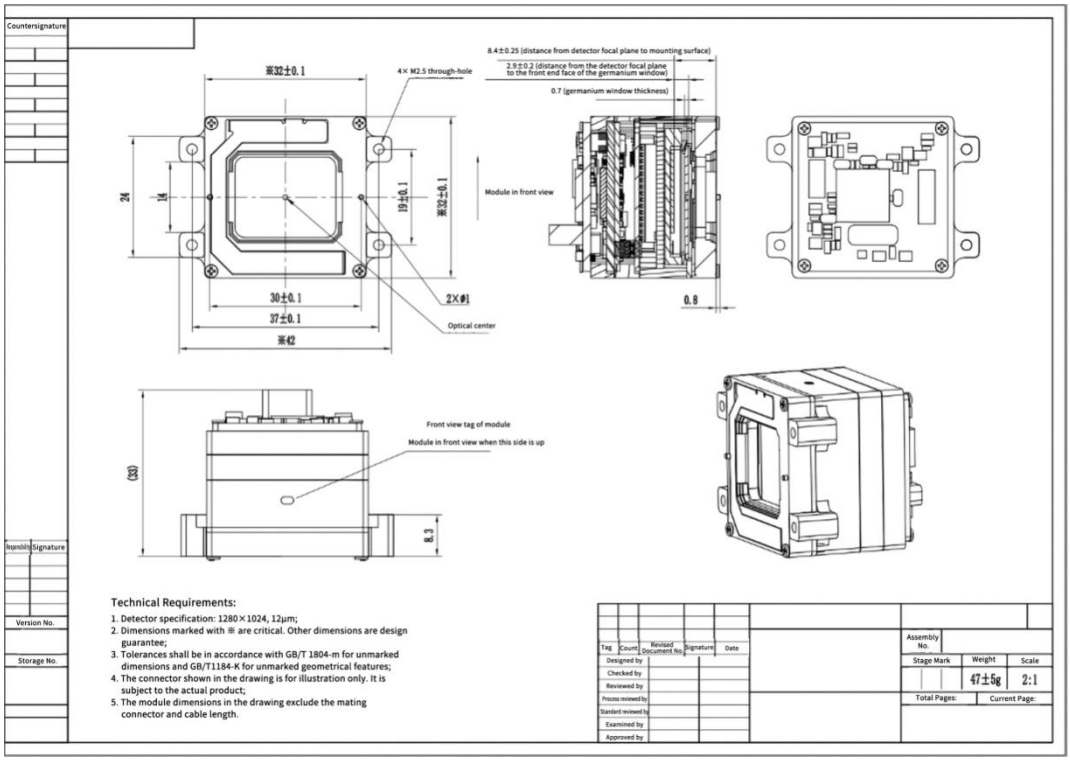


Figure 5.4 Module Structure with USB Extension Component

6 Precautions

To protect you and others from injury or to protect your equipment from damage, please read all the following information before using your equipment.

(1) The product shall not face towards the sun or other high-intensity radiation sources directly;

(2) The optimal environment temperature for operating is - 20 ℃ to 50 ℃;

(3) The detector window shall not be touched or hit with hands or other objects;

(4) The equipment and cables shall not be touched with wet hands;

(5) Please do not bend or damage cables;

(6) Scrubbing your equipment with diluents is prohibited;

(7) Do not unplug and plug cables when the power is on;

(8) Wrong cable should not be connected in case that brings damages to the equipment;

(9) Please pay attention to prevent static electricity;

(10) Please do not disassemble the equipment. If there is any fault, please contact us, and professional personnel will carry out maintenance.